SUMMARY

The invention relates to a data packet switching node to be used in an asynchronous digital network. This data packet switching node comprises:

- an input stage, cutting data packets into segments of constant length,
- a switching matrix having input ports and output ports supporting identical bit rates B switching the segments;
- and an output stage reconstructing the data packets from the segments supplied by the output ports of said switching matrix,

According to the invention, the input stage comprises at least one input interface with a bit rate equal to a multiple of B, ki*B, and means for splitting the data packet into ki input ports of the switching matrix. Moreover, the output stage comprises at least one output interface with a bit rate equal to a multiple of B, ko*B, and means for reconstructing a data packet with a bit rate equal to ko*B by concatenating segments supplied by ko output ports of said switching matrix where ki*ko>1.